A. CHEHAB
M. MANSOUR

FACULTY OF ENGINEERING AND ARCHITECTURE
AMERICAN UNIVERSITY OF BEIRUT
SUMMER 2010
MIDTERM

DIGITAL SYTEMS DESIGN (EECE320)

July 19, 2010

NAME: Sara Youssef ID: [redacted]

CLOSED BOOK (90 MINUTES)

CIRCLE THE NAME OF YOUR INSTRUCTOR

WRITE YOUR NAME AND ID NUMBER IN THE SPACE PROVIDED ABOVE.

CALCULATORS ARE NOT ALLOWED.

PROVIDE YOUR ANSWERS IN THE SPACE PROVIDED ON THE QUESTION SHEET.

THE SCRATCH BOOKLET WILL NOT BE CONSIDERED IN GRADING.

BE AS NEAT AND CLEAR AS POSSIBLE.

GOOD LUCK!

Problem	Total Points	Earned Points
1	20	18
2	4	4
3	6	3
4	6	5
5	6	5
6	8	6
7	8	7
8	8	8
9	6	3
10	6	4
11	12	11
12	10	10
Total	100	

84/100

Problem 1 (20 points)

a) The 10's complement of the decimal number 84091239 is: 15908761

b) Represent the following decimal numbers using two's complement with just enough bits:

+ 39 = (0100111)

- 21 = (101011)

c) Convert the following binary number to Octal and to Hexadecimal:

11011101010.001100 = (3352,14)$_8$

11011101010.00110 = (6EA,3)$_{16}$

d) Convert the hexadecimal number 7CE3B to Octal: 17163073

e) What is the minimum number of bits required to represent a binary code having 200 codewords?

Answer: 8

f) The decimal value of the unsigned binary number 101110.0111 is: 46,4375

g) Use DeMorgan's theorem to complement the following expression: F = X'Y'(Z+W) + X(Y+W)

Answer: $f' = (X+Y+ZW')\cdot(X+Y'W')$

h) What is the Π representation of $F = \sum_{w,x,y,z}(1,9,13,14)$?

Answer: $\Pi_{w,x,y,z}(0,2,3,4,5,6,7,8,10,11,12,15)$

i) The maximum decimal value to which a 3-digit, base-b adder can add is $124_{(10)}$. What is the value of b?

The base b = 5

j) The decimal number 753 is represented in Excess-3 code as: 1010 0110

10 8 6

0001 0000 1000 1100

Problem 2 (4 points)

Given F(A,B,C,D) = AB + A'C+D, express F as a product of MAXTERMS.

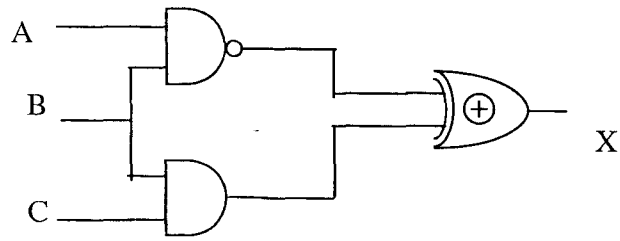
$(A+C)(B+A')(B+C)+D = (D+A+C)(D+B+A')(D+B+C)$

$= (D+A+C+B)(D+A+C+B')(D+B+A'+C)(D+B+A'+C')$
$(D+B+C+A)(D+B+C+A')$

4

Problem 3 (6 points)

Write the Boolean expression of the following circuit and reduce it using Boolean algebra. The expression should contain only AND, OR and NOT operations.



3

$X = AB \text{ XOR } (BC)$

$= AB(BC) + (AB)'(BC)'$

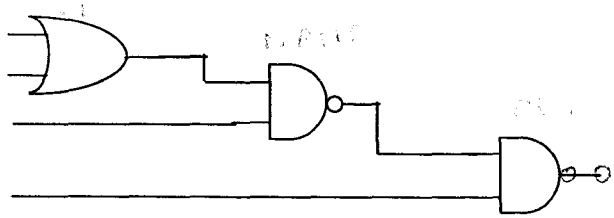
$= ABC + (AB+BC)'$

?

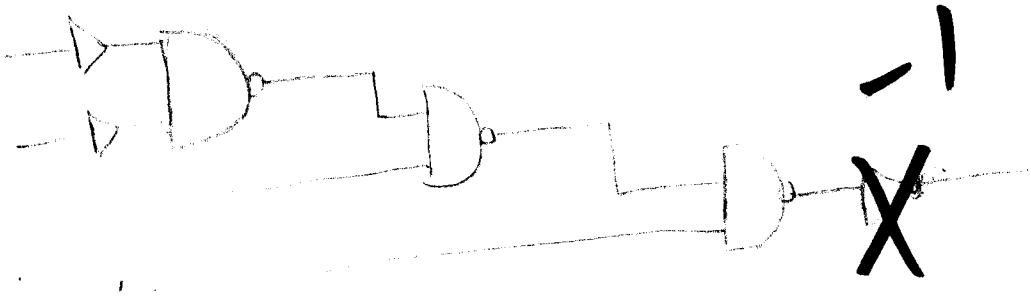
-3

Problem 4 (6 points)

Convert the following circuit into a circuit consisting of NAND and NOT gates only.



5



-1

Problem 5 (6 points)

Use the Karnaugh map to obtain a minimum **SOP** expression of the following logic function:

$F = \Sigma_{ABCD}(0, 5, 10, 15) + \Sigma d(3, 8, 13)$

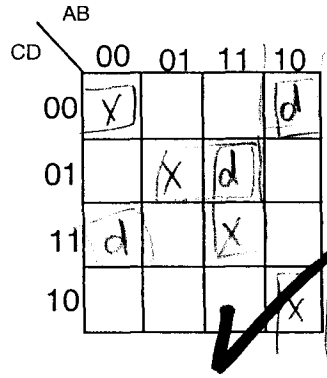
0101 0011 1101 1010 1000 1111

5

-1

F = B'C'D' + AB'D' + BC'D + AB

+ A'B'C



3

Problem 6 (8 points)

Consider the function: $F = \Sigma_{A,B,C,D}(0, 1, 2, 4, 5, 6, 7, 9, 11, 12, 13, 14)$

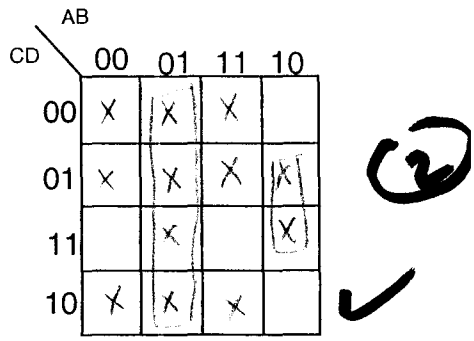
6

a) What are the essential prime implicants of F?

2 A'B and AB'D -2

b) What are the other prime implicants of F?

A'C', A'D', BC', BD', A'CD', BCD', C'D -2



2

Problem 7 (8 points)

For the following logic expression (F), indicate all the transitions that cause a static hazard in the corresponding two-level AND-OR circuit, and suggest a new expression for a hazard-free circuit that realizes the same logic function.

7

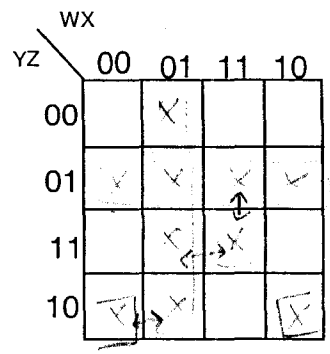
F = W'.X + Y'.Z + W.X.Y.Z + X'.Y.Z'

3

Transitions causing hazards are:

0111 ↔ 1111, 1101 ↔ 1111

0010 ↔ 0110



2

Hazard-Free F = W'X + Y'Z + WXYZ + XYZ'

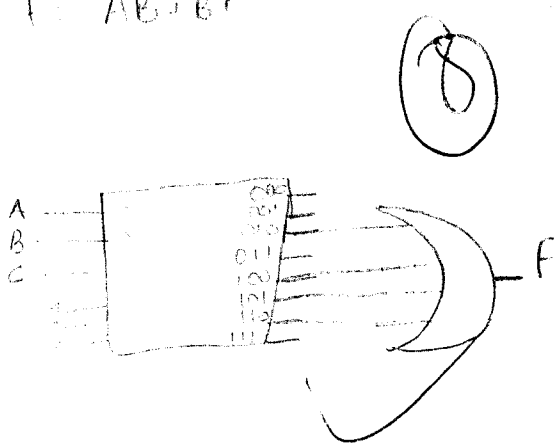
+ W'YZ' + X'YZ + WXZ

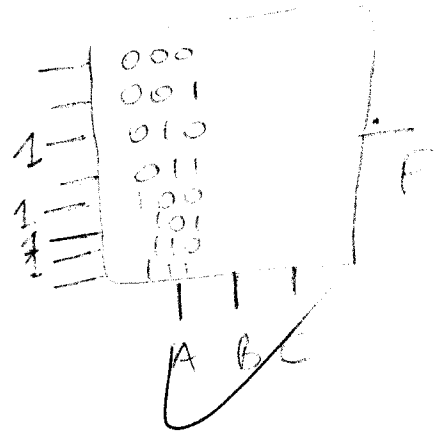
-1

2

Problem 8 (8 points)

Implement the function F = AB' + BC' using a 3-to-8 decoder (with additional gates). Implement it also using an 8-input multiplexer. Assume that A is the most significant bit.

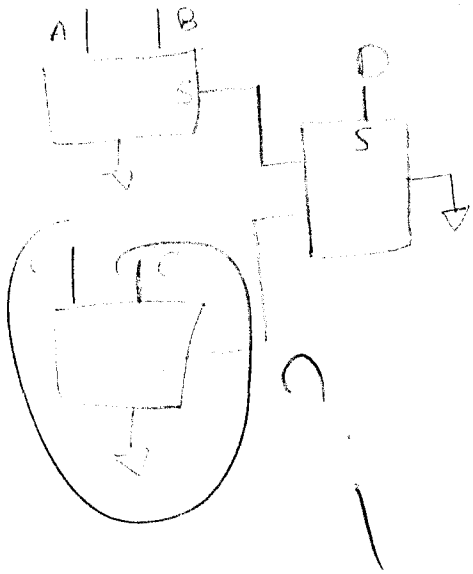


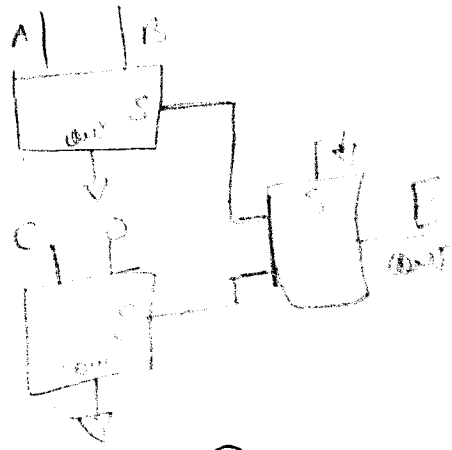


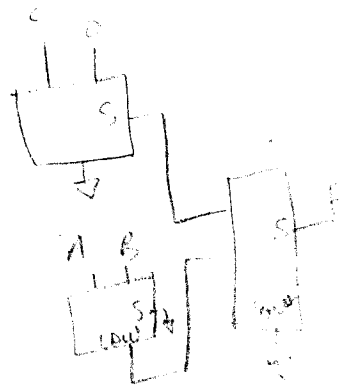
Problem 9 (6 points)

A half-adder adds only two bits (A and B, without carry-in) and produces two outputs, the sum (S) and carry (C). Find the expressions of S and C in terms of A and B and then implement the following four functions using three half adders. You have to show the inputs that are connected to each half adder and what are the outputs of the adders.

D = A ⊕ B ⊕ C E = A'BC + AB'C F = ABC' + (A'+B')C G = ABC



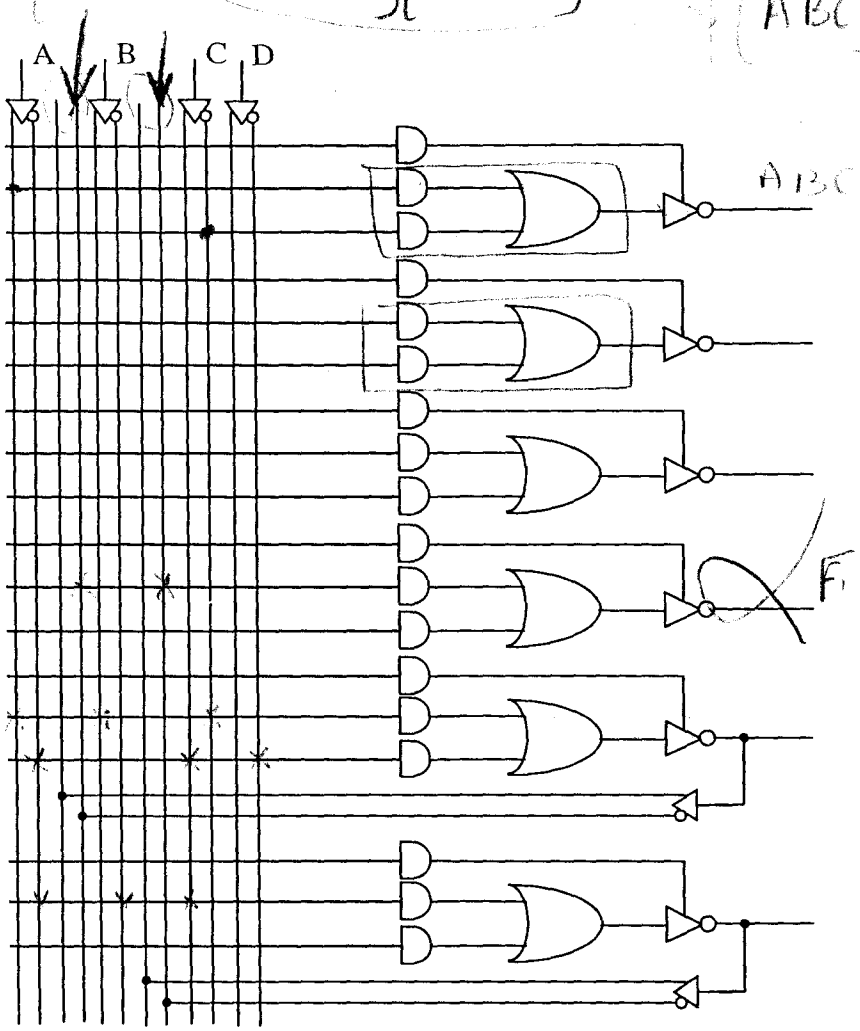




Problem 10 (6 points)

Implement the following function using the PAL4L6 shown below.

F1 = (A' + B' + C).(A + C' + D).(A + B + C')



Problem 11 (12 points)

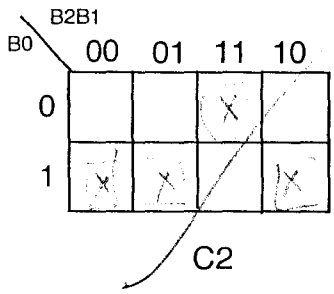
Design a circuit to **increment a 3-bit binary number in bit-reversed order**. The inputs are B0, B1 and B2, where B2 is the most significant digit and the outputs are C0, C1 and C2 where C2 is the most significant digit. The operation of this circuit is given by $C_2C_1C_0 = B_0B_1B_2 + 001$.

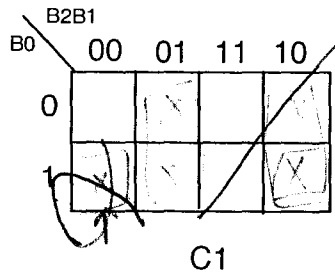
(i) Show a **truth table** for the circuit.

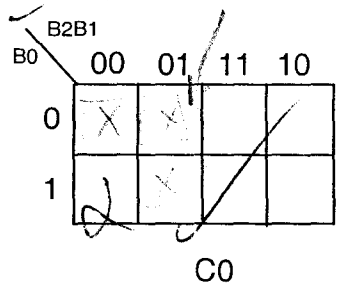
(ii) Draw **Karnaugh maps for each output** and use them to simplify the functions.

(iii) Draw a **schematic diagram** using the **minimum number of NAND gates and inverters only**.

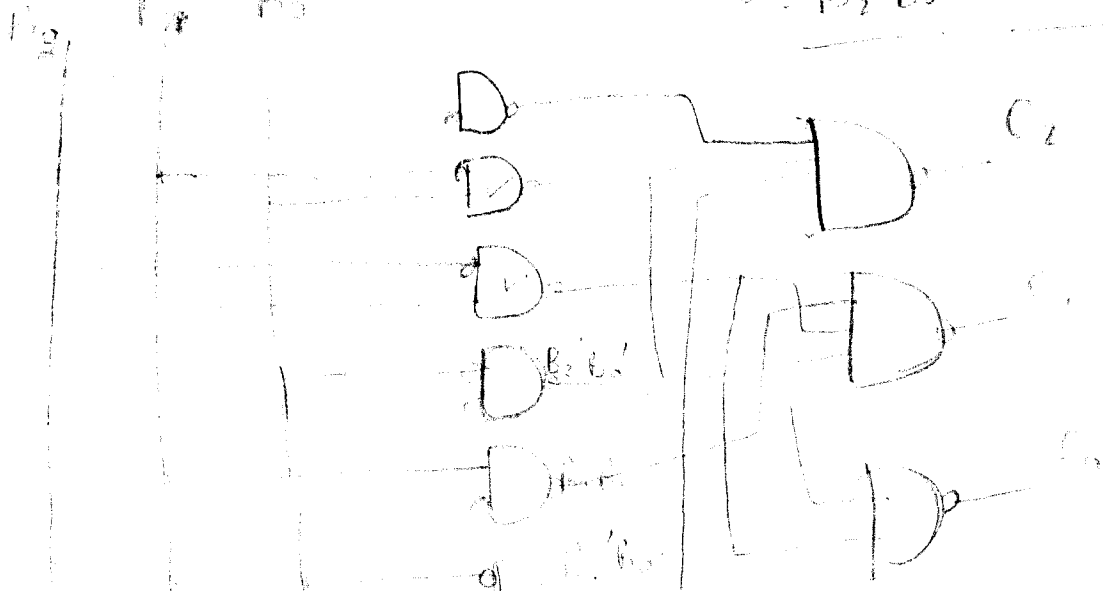
B2	B1	B0	C2	C1	C0
0	0	0	0	0	1
0	0	1	1	1	0
0	1	0	0	1	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	0	0	0







$C_2 = B_2'B_0 + B_1'B_0 + B_1B_0'$ $C_1 = B_2B_1' + B_2'B_1 + B_1B_0$ $C_0 = B_2'B_0' + B_2B_1'$



Problem 12 (10 points)

Write a VHDL entity and architecture to implement a 2-4 decoder with enable using the **behavioral style**. The decoder has an active-high enable signal (EN). Then, write a testbench to the test the decoder with 5 cases, one with enable low and 4 with enable high checking the 4 possibilities of the input lines.

```
entity encoder is
port ( A : in std_logic_vector (1 down to 0)
       EN : in std_logic
       B : out std_logic_vector (3 down to 0) );
end entity;

architecture S of encoder is
begin
process ( ) sensitivity ?
variable Y_s : std_logic_vector (3 down to 0);
CASE A is
when "00" => Y_s := "0001";
when "01" => Y_s := "0010";
when "10" => Y_s := "0100";
when "11" => Y_s := "1000";
others => Y_s := ...;
end case;
if (EN = '1') then B <= Y_s;
else B <= "0000";
end if;
end process;
end S;
```